In re Patent Application of:
MEARS ET AL.
Serial No. **10/647,061**
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In the Specification:

Please replace paragraph 0056 with the following rewritten paragraph:

FIG. 6E depicts the devices after the gate oxide layers **416** and the gates **418** are formed. To form these layers, a thin gate oxide is deposited, and steps of poly deposition, patterning, and etching are performed. Poly deposition refers to low pressure chemical vapor deposition (LPCVD) of silicon onto an oxide (hence it forms a polycrystalline material). The step includes doping with P+ or As- to make it conducting and the layer is around 250 nm thick.

Please replace paragraph 0058 with the following rewritten paragraph:

In FIG. 6F, lowly doped source and drain regions **420, 422** are formed adjacent the channels **424** and **426**. These regions are formed using n-type and p-type LDD implantation, annealing, and cleaning. "LDD" refers to n-type lowly doped drain, or on the source side, p-type lowly doped source. This is a low energy/low dose implant that is the same ion type as the source/drain. An anneal step may be used after the LDD implantation, but depending on the specific process, it may be omitted. The clean step is a chemical etch to remove metals and organics prior to depositing an oxide layer.

Please replace paragraph 0059 with the following rewritten paragraph:

FIG. 6G shows the spacer **428** formation and the source and drain implants. An SiO_2 mask is deposited and etched back. N-type and p-type ion implantation is used to form the source and drain regions **430, 432, 434,** and **436**. Then the structure is annealed and cleaned. FIG. 6H depicts the self-aligned silicides **438** formation, also known as salicidation. The salicidation process includes metal deposition (e.g. Ti), nitrogen annealing, metal etching, and a second annealing. This, of course, is just one example of a process and device in which the present invention may be used, and those of skill in the art will understand its application and use in many other processes and devices. In other processes and devices the structures of the present invention may be formed on a portion of a wafer or across substantially all of a wafer. In other processes and devices the structures of the present invention may be formed on a portion of a wafer or across substantially all of a wafer.